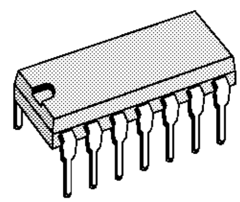
SGS-THOMSON MICROELECTRONICS

TDA4433

TV SIGNAL IDENTIFICATION CIRCUIT AND AFC INTERFACE

- IDENTIFICATION OF TRUE TV STATIONS ONLY
- LOW IMPEDANCE OUTPUT OF THE IDENTIFICATION SIGNAL
- DIGITAL CONTROL SIGNAL FOR AUTOMATIC SEARCH AND AFC OPERATION
- THERMAL COMPENSATION OF THE VOLTAGE REGULATOR



DIP14
(Plastic Package)

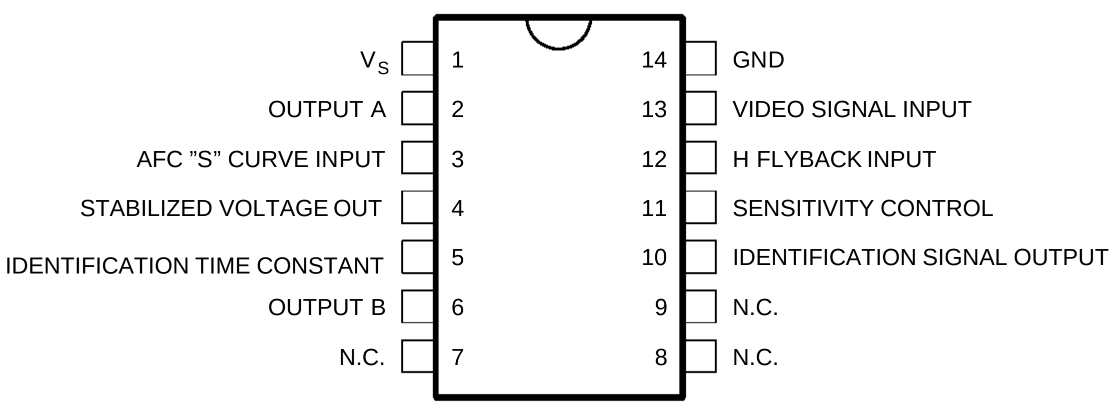
ORDER CODE : TDA4433

DESCRIPTION

The TDA4433 is a monolithic integrated circuit in a 14 lead dual-in-line plastic package. It integrates the following functions :

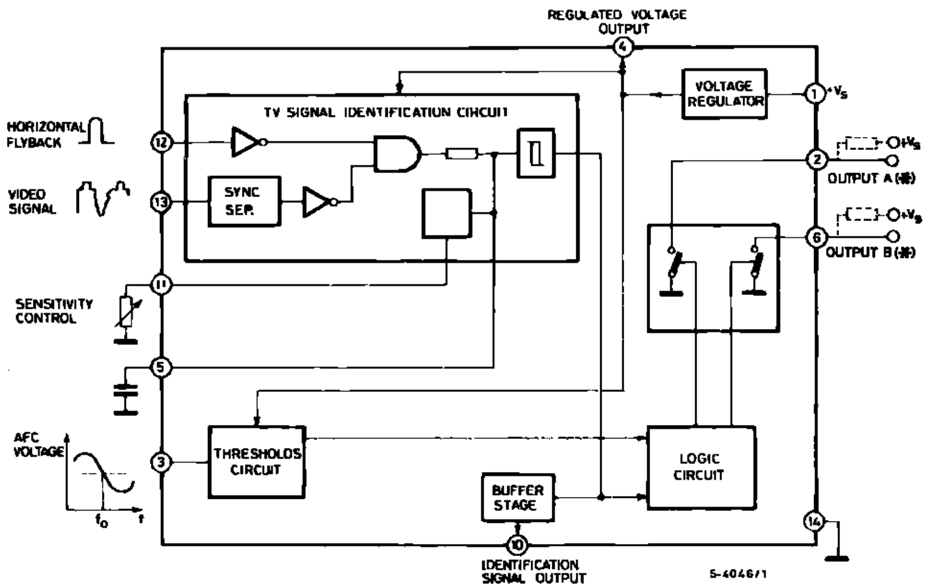
- TV signal identificator - Sync. separator - Threshold detector - Digital Interface - Voltage regulator.

PIN CONNECTIONS



4433-01.EPS

BLOCK DIAGRAM



* Open collector outputs

4433-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage (pin 1)	16	V
V_3	Voltage at Pin 3	16	V
V_{13}	Voltage at Pin 13	– 5, + 6	V
I_6 ; I_2	Pin 6 and Pin 2 Current	1	mA
I_{10}	Pin 10 Current	2	mA
I_{11}	Pin 11 Current	2	mA
I_{12}	Pin 12 Current	± 2	mA
P_{tot}	Total Power Dissipation at $T_{amb} \leq 70$ °C	800	mW
T_{stg}, T_j	Storage and Junction Temperature	– 40, +150	°C

4433-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	100	°C/W

4433-02.TBL

ELECTRICAL CHARACTERISTICS

(refer to the test circuit ; V_S = 12 V, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage Range (pin 1)		10.8		14.5	V
I_s	Supply Current (pin 1)	V_s = 14.5 V			30	mA
V_2	Output Voltage	$f_{tuning} < fo$ I_2 = 1 mA	V_s – 0.5			V
		$f_{tuning} = f_o$			0.8	V
		$f_{tuning} > f_o$			0.8	V
V_6	Output Voltage	$f_{tuning} < f_o$ I_6 = 1 mA			0.8	V
		$f_{tuning} = f_o$ I_6 = 1 mA			0.8	V
		$f_{tuning} > f_o$	V_s – 0.5			V

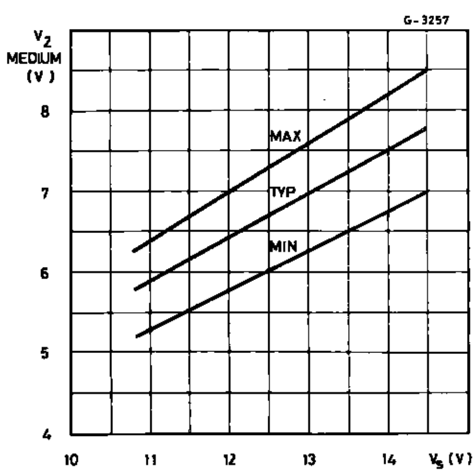
4433-03.TBL

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_3	Input Voltage Range		4		8	V
V_{3U}	Upper Threshold Voltage	See Figure 2	$V_4 - 25$	V_4	$V_4 + 25$	mV
V_{3L}	Lower Threshold Voltage	See Figure 2	$V_4 - 425$	$V_4 - 400$	$V_4 - 375$	mV
R_3	Input Resistance	$V_3 = V_4$	1.4			MΩ
V_4	Regulated Voltage	$I_4 = 1$ mA		6.6		V
I_4	Output Current				1	mA
R_4	Output Differential Resistance			60		Ω
$\frac{\Delta V_4}{\Delta T_S}$	Regulated Voltage Thermal Drift				± 2	mV/°C
V_{10}	Identification Output Voltage	No Identification, $I_{10} = 1$ mA	$V_s - 1.3$			V
		Identification			20	mV
R_{10}	Output Resistance			100		Ω
V_{12}	Switch off Threshold Voltage				1	V
I_{12}	Input Flyback Current		0.5		1.5	mA
R_{12}	Input Resistance	$V_{12} = 3$ V		10		kΩ
t_{fly}	Flyback Pulse Duration		10		17	µsec.
t	Time Delay between Leading Edges of Flyback Pulse and Sync. Pulse		0		3.5	µsec.
V_{13}	Video Input Signal (peak to peak)		2.5		4.5	V
V_{13}	Sync. Pulse Amplitude (above black level)		0.52			V
R_{13}	Input Resistance				1.5	kΩ

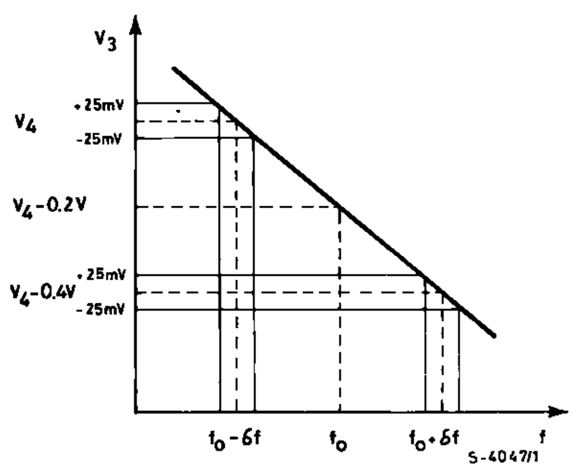
4433-04.TBL

Figure 1 : Medium Output Voltage vs. Supply Voltage



4433-03.EPS

Figure 2 : Digital AFC Threshold Voltage vs. Frequency

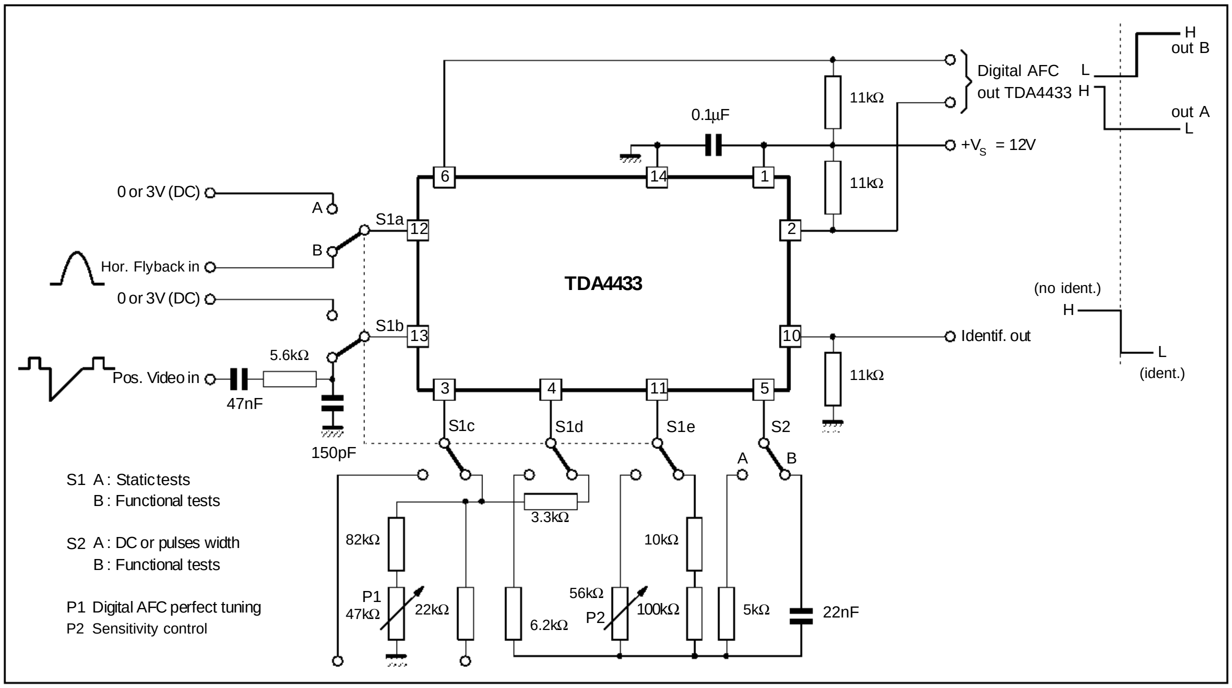


4433-04.EPS

Input Voltage (V_3)	Output Voltage (V_2)	Output Voltage (V_6)
$V_3 > V_4$	High level	Low Level
$V_4 - 0.4\ V < V_3 < V_4$	Low Level	Low Level
$V_2 < V_4 - 0.4\ V$	Low Level	High Level

4433-05.TBL

TEST CIRCUIT



4433-05.EPS

APPLICATION INFORMATION

(refer to the block diagram)

TV Signal Identification Circuit

The circuit recognizes only TV signals by checking logically during one line the coincidence between the horizontal flyback pulse and the pulse detected by a sync. separator.

The signal identification is carried out by charging the capacitor connected to pin 5 ; when the capacitor voltage overcomes a fixed threshold voltage, a Schmitt trigger switches and enables the AFC control. If a TV signal is recognized, the capacitor is slightly charged every line and its voltage reaches the threshold after a number of line which is defined by the value of the capacitor itself. The sensitivity of the identification circuit, hence the number of lines required to charge the capacitor, can be adjusted by means of the resistor connected between pin 11 and ground.

When the identification has been made, a signal (level L) is available at pin 10.

Threshold Circuit

The circuit detects 3 ranges of AFC voltage and in combination with the TV signal identification circuit drives the electronic switches.

With a correct TV signal, the output levels corresponding to the 3 ranges are :

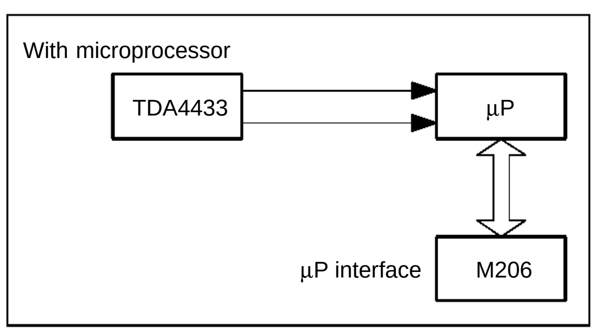
	(V_2)	**(V_6)**
$f_o - \delta f$	High Level	Low Level
f_o	Low Level	Low Level
$f_o + \delta f$	Low Level	High Level

The TDA4433 has two separate outputs which can have only two states, high (H) or low (L). The outputs at pin 2 and at pin 6 remain at a low level with no video signal input or with a video signal not identified as a true TV signal. Both pin 2 and pin 6 are open collector outputs and must be pulled-up to the positive supply voltage by external resistors.

Voltage Regulator

The circuit can deliver 1 mA and it can be used as D/A converter reference to supply fine tuning voltage.

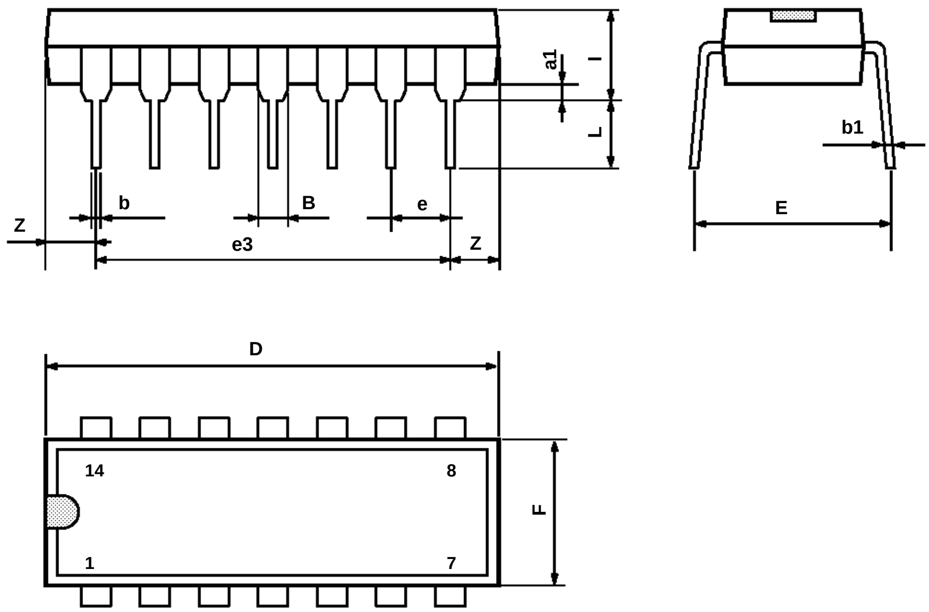
EPM SYSTEM CONFIGURATIONS



4433-05.EPS

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP



PM-DIP14.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

DIP14.TBL